polyimide is deposited over the passivation layers. This layer of photosensitive polyimide is patterned, exposed and developed, the passivation layer is patterned and etched to expose the underlying bonding pads. The remaining polyimide is cured and cross-linked and remains in place to serve as a buffer during further device packaging.

Claim rejections - 35 U.S.C. § 103(a)

Reconsideration of the rejection of claims 1-25 and 27-30 under 35 U.S.C 103(a) as being unpatentable over Fu (US Patent 5,807,787) in view of Yamamoto (US Patent 5,013,689) and further in view of Lukanc (US Patent 6,066,557) is respectfully requested based on the following arguments.

To facilitate the comparison of the instant invention with Fu in view of Yamamoto and Lukanc, the essential steps of the instant invention are summarized. The instant invention:

- starts with a semiconductor surface, typically the surface of a semiconductor substrate, over which a pattern of metal has been created, including interconnect lines and bonding pads
- a first layer of passivation is deposited over the semiconductor surface including the surface of the metal patterns

- a second layer of passivation is deposited over the first layer of passivation
- a thick layer of polyimide is deposited over the surface of the second layer of passivation
- the thick layer of polyimide is patterned and etched creating openings in the layer overlying the surface of the bonding pads, leaving the polyimide in place above the interconnect line pattern,
- the layers of passivation are etched, exposing the surface of the bonding pads, and
- the thick layer of polyimide is cured and cross-linked in order to provide improved protection for the interconnect metal.

Fu et al. follow the steps of:

- start with a semiconductor surface, typically the surface of a semiconductor substrate, over which a pattern of bonding pads has been created; Fu et al. use an insulation layer over which the metal patterns are created; it must be clearly noted at this time that Fu et al. do not address the creation of a pattern of interconnect lines, this is a key difference with the instant invention where (Fig. 8 and 9 of the instant

invention) interconnect lines 12 and a bond pad 14 are defined

- a first layer of passivation is deposited over the semiconductor surface including the surface of the bonding pads; this layer is typically between 7000 and 12000 Angstrom thick (col. 5, line 24); Fu et al. do not deposit two layers of passivation, one on top of the other; this is a key difference with the instant invention where (Fig. 8 and 9 of the instant invention) passivation layers 16 and 18 are defined
- openings are etched in the first layer of passivation, exposing the surface of the bonding pads (col. 5, lines 25); this is a key difference with the instant invention which does not etch an opening in the first or the second of both layers of passivation after these layers of passivation have been deposited; etching of the layers of passivation takes place under the instant invention after a layer of polyimide has been deposited and etched over the two layers of passivation
- a second layer of passivation is deposited, the second passivation layer is typically polyimide (col. 5, line 38), with a thickness between 9.0 and 12.0 um; this is a key difference with the instant invention where two layers of passivation (comprising PE oxide and PE silicon nitride and

not, in contrast with Fu et al., where polyimide is used for the second layer of passivation) are deposited one over the other without an intervening processing step of etching the first layer of passivation; the etching of the layers of passivation of the instant invention occurs at a later step in the process at which time both the layers of passivation are etched one after the other (see claim 1 of the instant invention); the second layer of passivation that is deposited by Fu et al. are deposited over the partially exposed surface of the bond pads; the layer of polyimide that is deposited under the instant invention does not touch any metal surface, which again is a key difference with Fu et al.; the layer of polyimide of the instant invention in fact "takes the place of" a layer of photoresist in creating openings to the bond pads; this offers a number of advantages that have been detailed in the specification of the instant invention, most notably among these advantages is that the polyimide, after etching and curing, can be left in place, forming a tough protective layer for the underlying interconnect lines (12, Figs 8, 9 of the instant invention); further polyimide provides the ability to withstand high temperatures without dielectric breakdown, simple processing requirements, they produce surfaces in which the step heights of underlying

features are reduced, step slopes which are gentle and smooth and an acceptable dielectric constant.

- the second layer of passivation is exposed to UV light resulting in cross linked polyimide (the polyimide that is exposed by the UV light) and polyimide (that is not exposed by the UV light) that can be dissolved away; this results in creating openings in the layer of polyimide that expose that surface of the contact pads (col. 5, lines 60-65)
- residual polyimide is removed by oxygen plasma ashing (col. 5, line 67), the residual polyimide caused problems of poor contact resistance with the bonding pads (col. 6, which 2) which in turn has a negative impact on product yield; the instant invention does not need to perform this processing step since, after the polyimide of the instant invention has been etched, the passivation layers are etched further removing any left over polyimide from the surface of the bond pad; and
- after the plasma ashing, the surface of the substrate is subjected to a thermal treatment to eliminate surface leakage currents (col. 6, lines 43 and 48).

The comparison between Fu et al. and the instant invention has been provided in a prior Office Action and therefore will not be repeated at this time. Applicant respectfully draws the

same conclusions that have been drawn as part of a previous Office Action, that is:

"In sum: both Fu et al. and the present invention use polyimide and apply heat treatment to the surface of the deposited polyimide. Other than that, there is no commonality between Fu et al. and the present invention. Fu et al. reduces leakage currents between bonding pads by creating a thick layer of polyimide between the bonding pads (under which one layer of passivation have been deposited and patterned to expose the bonding pads) and heat treating this layer of polyimide. The present invention creates a bonding pad that is adjacent to interconnect lines, uses two layers of passivation over the interconnect lines and provides low resistivity access to a bond pad concurrent with protection for the interconnect lines with a thick layer of polyimide."

It would not be obvious to combine the teachings of Yamamoto and Lukanc with those of Fu, since there is no suggestion or motivation in the teachings of any of the patents of the present invention. Contrary to the Examiner's assertion that Yamamoto discloses forming bonding pad windows, Yamamoto does not mention bond pads but provides a method for forming a passivation film for the protection of semiconductor circuits and/or circuit

elements on semiconductor chips. Applicant has carefully scrutinized Yamamoto cited by Examiner but fails to find any mention of forming bonding pad windows. Yamamoto does disclose forming a first passivation layer, forming an organic resist layer on the first passivation layer, forming windows in the layer of organic resist to expose the first layer of passivation and removing the exposed first layer of passivation, thus forming a two layer passivation film. Yamamoto specifies a number of materials that can be used for the two layer passivation film but here again is none of this connected with the creation of bonding pads.

Applicant has carefully reviewed the Yamamoto specification for any reference to the terms "bond pad" and/or "interconnect lines", in other words any references to creating a bond pad that is adjacent to a layer of interconnect lines and creating an opening to the bond pad and simultaneously providing a protective layer of cured polyimide over the surface of the adjacent interconnect lines. Applicant has failed to find any such reference. Further:

- Yamamoto does not provide a method for negating the effect introduced by key-holes between closely spaced lines; the present invention does

- Yamamoto does not provided a method for preventing damage to a second layer of passivation during the process of etching to expose underlying metal surfaces; the instant invention does
- Yamamoto does not provide for a thick layer of polyimide that acts as a protecting layer for underlying interconnect metal; the present invention does
- Yamamoto provides a thin protective organic layer on the surface of one or more layers of passivation, making the layer of passivation into a high quality layer of passivation; the invention uses a thick layer of polyimide on the surface of two layers of passivation for the protection of underlying interconnect lines, and
- Yamamoto is silent on creating bonding pads at the same time that interconnect lines are created; the present invention provides such a method.

Where specific processing parameters are cited by the instant invention, for instance claims 5-8, these conditions are added to limit and define the invention for the creation of the structure that is shown in cross section in Fig. 9 of the instant invention. It is considered of importance to provide this specification such that there is no doubt as to how the structure of Fig. 9 is created, most specifically the thick

layer of polyimide. For the creation of this thick layer of polyimide, it is also important to be specific on the creation of layers that are adjacent to the thick layer of polyimide, hence the specification for the first and second layers of passivation. The processing conditions for the creation of the thick layer of polyimide are basic to the creation of the structure of Fig. 10 and have therefore been made part of the specification.

Applicant has carefully reviewed the instant specification with the objective of finding a reference in this specification that relates the etching of a passivation layer with the processing that is applied to a barrier layer. This relating to Examiner's statement that Lukanc discloses applying a passivation layer onto a copper metallization structure. To the best of Applicant's knowledge, no reference has been made in the instant specification to the use of a barrier layer in any of the layers that are used by the invention. Barrier layers have found wide application in the creation of conductive openings and as an interface shield for deposited metal, most notably copper. The instant invention does not address any of these aspects of the semiconductor art. Metal barrier layers are typically deposited over the surface of an opening that is later filled with a metal conductor. There is a wide gap between using

a conventional metal barrier layer and equating this use with the use of a layer of polyimide to create a unique structure (Fig. 10 of the instant invention) with the objectives that have been documented in detail in the instant specification. A metal barrier layer has one purpose only that is to form a shield (or barrier) between metal deposited in an opening and a surrounding dielectric. It cannot be argued that the use of a barrier layer can be compared and equated with the thick layer of dielectric that is used as part of a invention, whereby the layer of polyimide provides additional advantages that have been highlighted in detail either in the subject specification or in a prior Office Action. It would become excessively redundant to again state these advantages at this time, such a recitation will therefore be refrained from at this time. This however does not make the points that have been stated as advantages of the use of the thick layer of polyimide of the invention any less valid or urgent, most certainly so if this thick layer of polyimide is equated with the use of a barrier layer in the creation of interconnect metal deposited in for instance damascene or dual damascene openings.

It would not be obvious to combine the teachings of Lukanc with Yamamoto and Fu, since there is no suggestion or motivation in the teachings of any of the patents of the present invention.

Contrary to the Examiner's assertion that Lukanc discloses applying a layer of passivation onto a copper metallization structure, Lukanc (Fig. 1B, layer 21) discloses depositing a layer of nitride over which a layer of insulation is deposited. In addition, both of these layers in addition are not deposited over copper metallization, as asserted by Examiner, but are deposited Fig. 1B, over interconnect pattern which at the time of deposition does not contain any metal. Lukans et al. prepare the layer of insulation, layer 23, Fig. 1B and Fig. 1E, for the deposition of a metal, such as copper, into the interconnect pattern by forming a layer (36, 37, Fig. 1E) of barrier material along the sidewalls of the opening through which the metal is deposited, thus providing for "fabricating protected copper metallization".

Lukanc et al. provide for the formation of protected copper metalization, providing the steps of:

- depositing a layer of dielectric over a semiconductor surface
- creating openings in the layer of dielectric, these openings being a dual damascene opening and a trench opening; the dual damascene opening overlays and exposes the surface of an interconnect line

- next are sequentially deposited a layer of nitride, a layer of insulating material
- a layer of photoresist is deposited over the surface of the layer of insulating material. The layer of photoresist is patterned and etched, creating openings in the layer of photoresist that align with the openings created in the layer of dielectric
- the layer of insulating material is etched in accordance with the openings created in the layer of photoresist, using the layer of nitride as an etch stop layer
- the patterned layer of photoresist is removed exposing the surface of the layer of insulating material, a barrier layer is deposited over the layer of insulating material including the inside surfaces of the openings created in the layer of insulating material
- the barrier layer is etched, removing the barrier layer from the bottom of the openings created in the layer of insulating material, further removing the barrier layer from the surface of the layer of insulating material, exposing the openings that have been created in the layer of dielectric.

After this latter step, a layer of barrier material remains in place on the sidewalls of the openings that have been created

in the layer of insulation. These remaining layers of barrier material serve as the protective barrier layer for the copper metal that is deposited in the openings that have been created in the layer of dielectric and the layer of insulating material. The cross section of the structure that is created by Lukanc et al., Fig. 1E, shows that a protective barrier layer has been formed which lines a via opening or a contact hole opening, the openings expose underlying conductive features (in the form of a trench and a dual damascene opening).

The instant invention does not address the creation of a protective barrier layer that lines openings to conductive features. In none of the drawings, specification or claims of the instant invention is the aspect of protective barrier layer addressed. For this reason, among others, is the processing sequence of the instant invention and the processing sequence as provided by Lukanc et al. considerably different:

- the instant invention does not start with a layer of dielectric in which trenches and dual damascene openings are created for interconnect feature; the instant invention starts with a semiconductor surface over which interconnect metal, comprising interconnect lines and a bond pad, have been created

- Lukanc et al. do not deposit a two layered protective layer of passivation, comprising PE oxide and PESi_3N_4, over the surface of interconnect metal since Lukanc et al. do not as part of their invention provide interconnect metal nor provide a means for protecting underlying interconnect metal
- Lukanc et al. do not provide for the deposition of a thick layer of photosensitive polyimide since the objective of Lukanc et al. in not in accordance with (does not require) such a layer of photosensitive polyimide
- Lukanc et al. do not create an opening that aligns with a contact pad while a thick layer of photosensitive polyimide is in place to protect (closely spaced) interconnect lines that are adjacent to a contact pad
- Lukanc et al. do not address preventing the accumulation of impurities between closely spaced interconnect lines
- Lukanc et al. are silent on curing and cross linking a layer of photosensitive polyimide since no such layer is used by Lukanc et al.
- Lukanc et al. are silent on etching a deposited layer of passivation after a thick layer of polyimide has been etched, thereby protecting adjacent interconnect lines during the etching of the layer of polyimide

- Lukanc et al. are silent on the deposition of two overlying layers of passivation, a first layer comprising PE oxide and a second layer comprising Plasma Enhanced Si_3Ni_4; this because Lukanc et al. have no need for such a layer while this layer is required by the instant invention in order to provide adequate protection for underlying layers during the etch of the thick layer of photosensitive polyimide
- Lukanc et al. are silent on using a layer of polyimide to serve as the masking layer for patterning a bond pad, the instant invention uses a layer of polyimide instead of a Prior Art layer of photoresist to define a bond pad; the etched layer of polyimide remains in place in contrast with prior art methods whereby an etched layer of photoresist must be removed
- Lukanc et al. are silent on exposing a layer of polyimide to UV light to define a bond pad, and the removal of the unexposed polyimide to expose the surface of a bond pad
- Lukanc et al. do not provide the advantage of leaving in place a layer of passivation that is well protected by a layer of cross-linked thick polyimide, the layer of passivation will therefore not be damaged by additional plasma etching

- Lukanc et al. do not provide the advantage that no stripping of photoresist is required after etching for the exposure of a bond pad since the instant invention leaves the thick layer of polyimide in place to serve as a stress buffer during packaging operations.

In short: where Lukanc et al. provide for a barrier layer that remains in place on the sidewalls of an opening that aligns with underlying interconnect openings for the creation of copper based interconnect metal, the instant invention provides for a considerably different process as highlighted above, the advantages and differences having been highlighted above.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-25 and 27-30 under 35 U.S.C 103(a) as being unpatentable over Fu (US Patent 5,807,787) in view of Yamamoto (US Patent 5,013,689) and further in view of Lukanc (US Patent 6,066,557) be withdrawn.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

SUMMARY

The invention teaches the deposition of a pattern of interconnecting lines and bond pads. Passivation layers are deposited over this metal pattern. A layer of photosensitive polyimide is deposited over the passivation layers. This layer of photosensitive polyimide is patterned, exposed and developed, the passivation layer is patterned and etched to expose the underlying bonding pads. The remaining polyimide is cured and cross-linked and remains in place to serve as a buffer during further device packaging.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 914-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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